ELEC 6200 PROJECT

PART 6 REPORT

Submitted By

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1. The project taught us designing and implementing CPU designs. We developed familiarity with Modelsim and Quartus. We also used Altera FPGA Boards in part 5. We now understand the different steps involved in designing a multi-cycle data path. Also, we learned how to simulate our processor on the Altera FPGA board provided in the lab.
2. We would probably to a pipeline data path if we got a chance to work on this project again.
3. Suggestions: Start working on the project at the earliest possible and make sure you design each and every component carefully.You do not want to spend time again working on the same components later if it doesn’t work. It takes forever to figure out what went wrong with the design. Our TA was very helpful and it would really help if you consulted your TA if you have any questions.